10-16-00 · EK287384616US
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
Docket No. **AUS9-2000-0390-US1**

Assistant Commissioner for Patents
Washington, D.C. 20231
Sir:

Transmitted herewith for filing is the patent application of Inventor(s):
Tam D. Bui, Chetan Mehta, Keng-Hiup Ng,
Jayeshkumar M. Patel, Amir Simon and Kiet Anh Tran

For: **A METHOD OF SYNCHRONIZING MULTIPLE NETWORKS USING
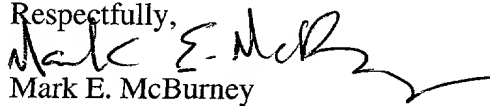PERMANENT ADDRESSING SCHEME**

Enclosed are also:

X	12	Pages of Specification including an Abstract
X	4	Pages of Claims
X	3	Sheet(s) of Drawings
X		A Declaration and Power of Attorney
X		Form PTO 1595 and assignment of the invention to IBM Corporation

CLAIMS AS FILED

FOR	Number Filed		Number Extra		Rate		Basic Fee ($710)
Total Claims	24	-20 =	4	X	$ 18	=	$ 72.00
Independent Claims	3	-3 =	0	X	$ 80	=	$ 00.00
Multiple Dependent Claims	0			X	$270	=	$ 00.00
				Total Filing Fee		**=**	**$ 782.00**

__X__   Please charge $782.00 to IBM Corporation, Deposit Account No. 09-0447.
__X__   The Commissioner is hereby authorized to charge payment of the following fees
associated with the communication or credit any over payment to IBM Corporation,
Deposit Account No. 09-0447. A duplicate copy of this sheet is enclosed.
    X   Any additional filing fees required under 37CFR § 1.16.
    X   Any patent application processing fees under 37CFR § 1.17.

Respectfully,

Mark E. McBurney
Reg. No. 33,114
Intellectual Property Law Dept.
IBM Corporation
11400 Burnet Road 4054
Austin, Texas 75758
Telephone: (512) 823-1003

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A METHOD OF SYNCHRONIZING MULTIPLE NETWORKS USING PERMANENT ADDRESSING SCHEME

5 ## BACKGROUND OF THE INVENTION

1. Technical Field:

The present invention relates to the field of computer software and, more particular, to management of
10 devices, node, and/or expansion tower addresses within a data processing system.

2. Description of Related Art:

Many computers that are used as servers, such as,
15 for example, as a server to host web pages, are multi-processor, multi-bus systems. These computers are capable of handling several tasks at once and performing each task very rapidly. These computers may also contain numerous input and output devices which are contained in
20 input/output (I/O) drawers. Each I/O drawer may contain, for example, up to 14 PCI adapters to allow devices, such as, for example, CDROMS, disk drives, and network adapters, to be connected to the computer.

These I/O drawers are typically physically separated
25 from the processors and memory components of the computer and are powered from a separate power supply. The I/O drawers and their components are connected to the main computer using varying types of cables, such as, for example, system power control network (SPCN) cables and
30 remote input/output (RIO) network cables which allow the I/O devices contained within the I/O drawers to function with the remainder of the computer as if they were on the

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system bus even if these devices are up to approximately fifteen feet away from the main computer.

One problem with using two or more physical networks, such as the SPCN and RIO networks mentioned

5 above, is that each network assigns its own unique address to each I/O drawer. This may not seem like a major problem on the surface, but, when an error occurs, it becomes difficult for a user to identify the correct drawer(s) and/or device(s) for replacement without

10 physically checking the RIO network connection or the SPCN network connection. Since, many of computers of this type may contain hundreds of I/O devices, finding the offending drawer(s) and/or device(s) in this manner can become quite time consuming and tedious. Therefore,

15 it would be desirable to have a method and system for synchronizing the two different physical network addresses such that the SPCN network and the RIO network use identical addresses to identify the same I/O drawer or node and also, the devices in that drawer.

20

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SUMMARY OF THE INVENTION

5   The present invention provides, a method, system, and apparatus for synchronizing device, node, and drawer addresses between two networks within a data processing system. In one embodiment, a service processor assigns a plurality of SPCN addresses to each of a plurality of

10   devices in the data processing system. System firmware then determines the RIO addresses corresponding to the plurality of devices. If one of the SPCN addresses is not the same as the RIO address for the corresponding device, node, or drawer, then the service processor

15   reassigns a new SPCN address to the corresponding device, node, or drawer such that the new SPCN address is identical to the RIO address for a corresponding device, node, or drawer.

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BRIEF DESCRIPTION OF THE DRAWINGS

5

The novel features believed characteristic of the invention are set forth in the appended claims. The invention itself, however, as well as a preferred mode of use, further objectives and advantages thereof, will best

10 be understood by reference to the following detailed description of an illustrative embodiment when read in conjunction with the accompanying drawings, wherein:

Figure 1 depicts a block diagram of a data processing system in which the present invention may be

15 implemented;

Figure 2 depicts a block diagram of a system for managing a system I/O drawers connected to multiple networks in accordance with the present invention; and

Figure 3 depicts a flowchart illustrating an

20 exemplary method of synchronizing addresses for multiple physical networks in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

5

With reference now to the figures, and in particular
with reference to **Figure 1**, a block diagram of a data
processing system in which the present invention may be
implemented is depicted. Data processing system **100** may

10   be a symmetric multiprocessor (SMP) system including a
plurality of processors **101**, **102**, **103**, and **104** connected
to system bus **106**. For example, data processing system
100 may be an IBM RS/6000, a product of International
Business Machines Corporation in Armonk, New York,

15   implemented as a server within a network. Alternatively,
a single processor system may be employed. Also
connected to system bus **106** is memory controller/cache
108, which provides an interface to a plurality of local
memories **160-163**. I/O bus bridge **110** is connected to

20   system bus **106** and provides an interface to I/O bus **112**.
Memory controller/cache **108** and I/O bus bridge **110** may be
integrated as depicted.

An RIO Controller **140** provides an interface between
processors **101-104** and local memories **160-163** with I/O

25   drawers **144-150**. I/O drawers **144-150** collectively
comprise an expansion tower. I/O drawers **144-150** are
powered independently from the rest of the data
processing system containing the processors **201-204** and
memory **160-163**. Connection between the I/O drawers

30   **144-150** and RIO Controller is made through buses **180-185**
as depicted which consist of cables including System

Power Control Network (SPCN), Remote Input Output (RIO) cables, JTAG buses, and operator panel cables. Bus **180** provides a connection between node 0 of RIO Controller **140** and I/O drawer **144** which is in turn connected to I/O

5 Drawer **146** through bus **181**. A return bus **182** connects I/O Drawer **146** to node 1 of RIO Controller **140**. Similarly, buses **183-185** are used to connect I/O drawer **148** and **150** to nodes 2 and 3 of RIO Controller **140**. Each I/O Drawer **144-150** holds up to 14 PCI I/O adapters. Four

10 succinct PCI buses are present in each of I/O drawers **144-150**. Each of I/O drawers **144-150** provides space for up to four media devices, such as, for example, tape drives, CDROM drives, and diskette drives, and two DASD bays each holding up to six disk drives.

15   A PCI host bridge **130** provides an interface for a PCI bus **131** to connect to I/O bus **112**. PCI bus **131** connects PCI host bridge **130** to the service processor mailbox interface and ISA bus access pass-through logic **194** and EADS **132**. The ISA bus access pass-through logic

20 **194** forwards PCI accesses destined to the PCI/ISA bridge **193**. The NV-RAM storage is connected to the ISA bus **196**. The Service processor **135** is coupled to the service processor mailbox interface **194** through its local PCI bus **195**. Service processor **135** is also connected to

25 processors **101-104** via a plurality of JTAG/I^{2}C buses **134**. JTAG/I^{2}C buses **134** are a combination of JTAG/scan busses (see IEEE 1149.1) and Phillips I^{2}C busses. However, alternatively, JTAG/I^{2}C buses **134** may be replaced by only Phillips I^{2}C busses or only JTAG/scan busses. All

30 SP-ATTN signals of the host processors **101**, **102**, **103**, and

104 are connected together to an interrupt input signal
of the service processor. The service processor **135** has
its own local memory **191**, and has access to the hardware
op-panel **190**.

5   Those of ordinary skill in the art will appreciate
that the hardware depicted in **Figure 1** may vary. For
example, other peripheral devices, such as optical disk
drives and the like, also may be used in addition to or
in place of the hardware depicted. The depicted example

10   is not meant to imply architectural limitations with
respect to the present invention.

       With reference now to **Figure 2**, a block diagram of a
system for managing a system I/O drawers connected to
multiple networks is depicted in accordance with the

15   present invention. System **200** may be implemented within
a data processing system such as, for example, data
processing system **100** in **Figure 1**. As discussed above, a
system I/O drawer is a modular component for inserting
I/O expansion slots into a data processing system. An

20   I/O drawer physically packages several PCI Host Bridges
(PHBs) to provide PCI I/O slots for plug-in I/O adapters.
System **200** includes four I/O drawers **202-208**, such as,
for example, I/O drawers **144-150** in **Figure 1**. However,
although depicted with four I/O drawers **202-208**, one

25   skilled in the art will recognize that more or fewer I/O
drawers may be included than depicted in **Figure 2**. It
should also be noted that some of I/O drawers **202-208** may
be connected to service processor **201** through RIO
networks only, through SPCN buses only, or through both.

30   The RIO Controller through which I/O drawers **202-208**

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would be connected to service processor **201** is not shown
for clarity. Also not shown are the various connections
between I/O drawers **202-208** with each other.

5   During the boot process, service processor **201**,
which may be implemented, for example, as service
processor **135** in **Figure 1**, assigns a unique SPCN ID to
each of I/O drawers **202-208** within the system **200** and
write this SPCN ID to SPCN config Table **224** in NVRAM **222**.
Service processor **201** uses the SPCN portion of SPCN & RIO
10   buses **280** to detect and assign unique IDs to I/O drawers
202-208, to control the power logic of the I/O drawers
202-208, and to monitor their environmental sensors such
as drawer temperature, fan speed, etc. NVRAM **222** may be
implemented as, for example, NVRAM **192** in **Figure 1**.
15   Once the SPCN addresses have been created and
written to SPCN config table **224**, the boot process
continues and system firmware **226** reads the SPCN config
table **224** information from NVRAM **222**. The system
firmware **226** then collects the RIO network address for
20   each of I/O drawers **202-208** connected via the RIO
network. Firmware **226** will then fill up SPCN Config
Table **224** with the RIO network drawer addresses and write
the modified SPCN config table to NVRAM **222**. If any
drawer address in SPCN config table does not match a
25   respective RIO drawer address, firmware **226** sends mailbox
to service processor **201** to assign a new drawer address
to any drawer address in the SPCN config table **224** that
doe not match with a respective RIO drawer address.
Service processor **201** will then assign a new permanent
30   SPCN drawer address to those drawers having an RIO drawer

address that does not match the SPCN drawer address.
After this point, both networks will identify the same
drawer or node with the same address or location.

5 Those of ordinary skill in the art will appreciate
that the components depicted in **Figure 2** may vary. For
example, more or fewer I/O drawers may be utilized than
depicted. The depicted example is not meant to imply
architectural limitations with respect to the present
invention.

10 With reference now to **Figure 3**, a flowchart
illustrating an exemplary method of synchronizing
addresses for multiple physical networks is depicted in
accordance with the present invention. Once the system
is powered on (step **302**), the service processor generates
15 an SPCN configuration table with all the drawers in the
system and writes it to the non-volatile random access
memory (NVRAM) (step **304**). The service processor ensures
that each drawer connected via the SPCN network has a
unique permanent address (step **306**). The data processing
20 system then continues with the system initialization
(boot) and system firmware reads the SPCN configuration
table information from NVRAM (step **308**).

System firmware then collects all of the RIO network
addresses for each drawer connected via the RIO network
25 (step **310**) and fills up the SPCN configuration table with
RIO network drawer addresses (step **312**). The firmware
then writes the modified SPCN config table to NVRAM (step
314). Next, it is determined whether all I/O drawer
addresses match (step **316**). If all drawer addresses
30 match between the SPCN network and the RIO network, then
the process is completed. If, however, all of the

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addresses do not match, then the firmware sends a mailbox to the service processor to assign a new drawer address to those I/O drawers whose SPCN address did not match the RIO address (step **318**). The service processor then

5 assigns a new permanent SPCN drawer address to the appropriate drawers such that the SPCN address and the RIO address for the corresponding I/O drawer are identical (step **320**).

It should be noted that although the present

10 invention has been described primarily with reference to matching addresses for I/O drawers for SPCN and RIO networks, other networks of drawers with two systems accessing the same drawers could be utilized as well. Also, while described primarily with reference to a

15 single expansion tower with four I/O drawers, more or fewer expansion towers and/or I/O drawers may be utilized than described herein.

It is important to note that while the present invention has been described in the context of a fully

20 functioning data processing system, those of ordinary skill in the art will appreciate that the processes of the present invention are capable of being distributed in the form of a computer readable medium of instructions and a variety of forms and that the present invention

25 applies equally regardless of the particular type of signal bearing media actually used to carry out the distribution. Examples of computer readable media include recordable-type media such a floppy disc, a hard disk drive, a RAM, and CD-ROMs and transmission-type

30 media such as digital and analog communications links.

The description of the present invention has been

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presented for purposes of illustration and description,
but is not intended to be exhaustive or limited to the
invention in the form disclosed. Many modifications and
variations will be apparent to those of ordinary skill in
5   the art. The embodiment was chosen and described in
order to best explain the principles of the invention,
the practical application, and to enable others of
ordinary skill in the art to understand the invention for
various embodiments with various modifications as are
10   suited to the particular use contemplated.

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CLAIMS:

What is claimed is:

5   1.   A method of synchronizing device addresses between
two networks within a data processing system, the method
comprising:

assigning a plurality of first unique addresses to
each of a plurality of devices for a first network;

10   determining a plurality of second unique addresses
for each of the plurality of devices for a second
network; and

responsive to a determination that one of the
plurality of first unique addresses is not identical to a

15   corresponding one of the plurality of second unique
addresses, reassigning a new unique address for the
corresponding one of the plurality of devices such that
the new unique address is identical to the corresponding
one of the plurality of second unique addresses.

20

2.   The method as recited in claim 1, wherein the device
is an input/output drawer.

3.   The method as recited in claim 1, wherein the device

25   is expansion tower.

4.   The method as recited in claim 1, wherein the first
unique address corresponds to an SPCN system address.

30   5.   The method as recited in claim 1, wherein the second
unique address corresponds to an RIO system address.

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6. The method as recited in claim 1, wherein the device is a CD-ROM drive.

5 7. The method as recited in claim 1, wherein the device is a DVD ROM drive.

8. The method as recited in claim 1, wherein the device is a hard drive.

10

9. A computer program product in a computer readable media for use in a data processing system for synchronizing device addresses between two networks within a data processing system, the computer program

15 product comprising:

first instructions for assigning a plurality of first unique addresses to each of a plurality of devices for a first network;

second instructions for determining a plurality of

20 second unique addresses for each of the plurality of devices for a second network; and

third instructions, responsive to a determination that one of the plurality of first unique addresses is not identical to a corresponding one of the plurality of

25 second unique addresses, for reassigning a new unique address for the corresponding one of the plurality of devices such that the new unique address is identical to the corresponding one of the plurality of second unique addresses.

30

10. The computer program product as recited in claim 9,

wherein the device is an input/output drawer.

11. The computer program product as recited in claim 9, wherein the device is expansion tower.

5

12. The computer program product as recited in claim 9, wherein the first unique address corresponds to an SPCN system address.

10   13. The computer program product as recited in claim 9, wherein the second unique address corresponds to an RIO system address.

14. The computer program product as recited in claim 9, 15   wherein the device is a CD-ROM drive.

15. The computer program product as recited in claim 9, wherein the device is a DVD ROM drive.

20   16. The computer program product as recited in claim 9, wherein the device is a hard drive.

17. A system for synchronizing device addresses between two networks within a data processing system, the system 25   comprising:

first means for assigning a plurality of first unique addresses to each of a plurality of devices for a first network;

second means for determining a plurality of second 30   unique addresses for each of the plurality of devices for a second network; and

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third means, responsive to a determination that one
of the plurality of first unique addresses is not
identical to a corresponding one of the plurality of
second unique addresses, for reassigning a new unique
5   address for the corresponding one of the plurality of
devices such that the new unique address is identical to
the corresponding one of the plurality of second unique
addresses.

10   18.   The system as recited in claim 17, wherein the
device is an input/output drawer.

19.   The system as recited in claim 17, wherein the
device is expansion tower.

15

20.   The system as recited in claim 17, wherein the first
unique address corresponds to an SPCN system address.

21.   The system as recited in claim 17, wherein the
20   second unique address corresponds to an RIO system
address.

22.   The system as recited in claim 17, wherein the
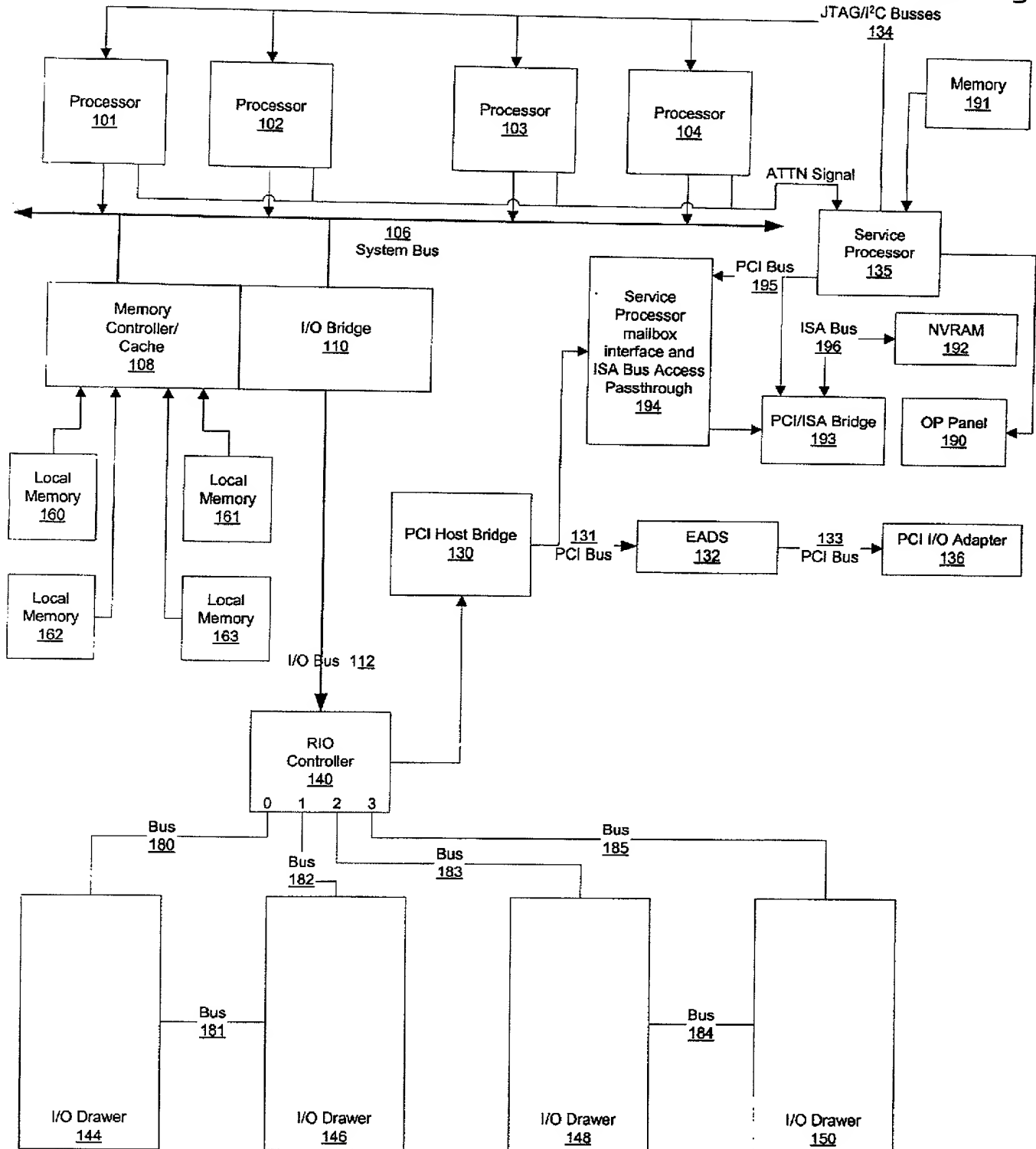device is a CD-ROM drive.

25

23.   The system as recited in claim 17, wherein the
device is a DVD ROM drive.

24.   The system as recited in claim 17, wherein the
30   device is a hard drive.

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ABSTRACT OF THE DISCLOSURE

A METHOD OF SYNCHRONIZING MULTIPLE NETWORKS USING PERMANENT ADDRESSING SCHEME

5

A method, system, and apparatus for synchronizing device, node, and drawer addresses between two networks within a data processing system is provided. In one embodiment, a service processor assigns a plurality of
10 SPCN addresses to each of a plurality of devices in the data processing system. System firmware then determines the RIO addresses corresponding to the plurality of devices. If one of the SPCN addresses is not the same as the RIO address for the corresponding device, node, or
15 drawer, then the service processor reassigns a new SPCN address to the corresponding device, node, or drawer such that the new SPCN address is identical to the RIO address for a corresponding device, node, or drawer.
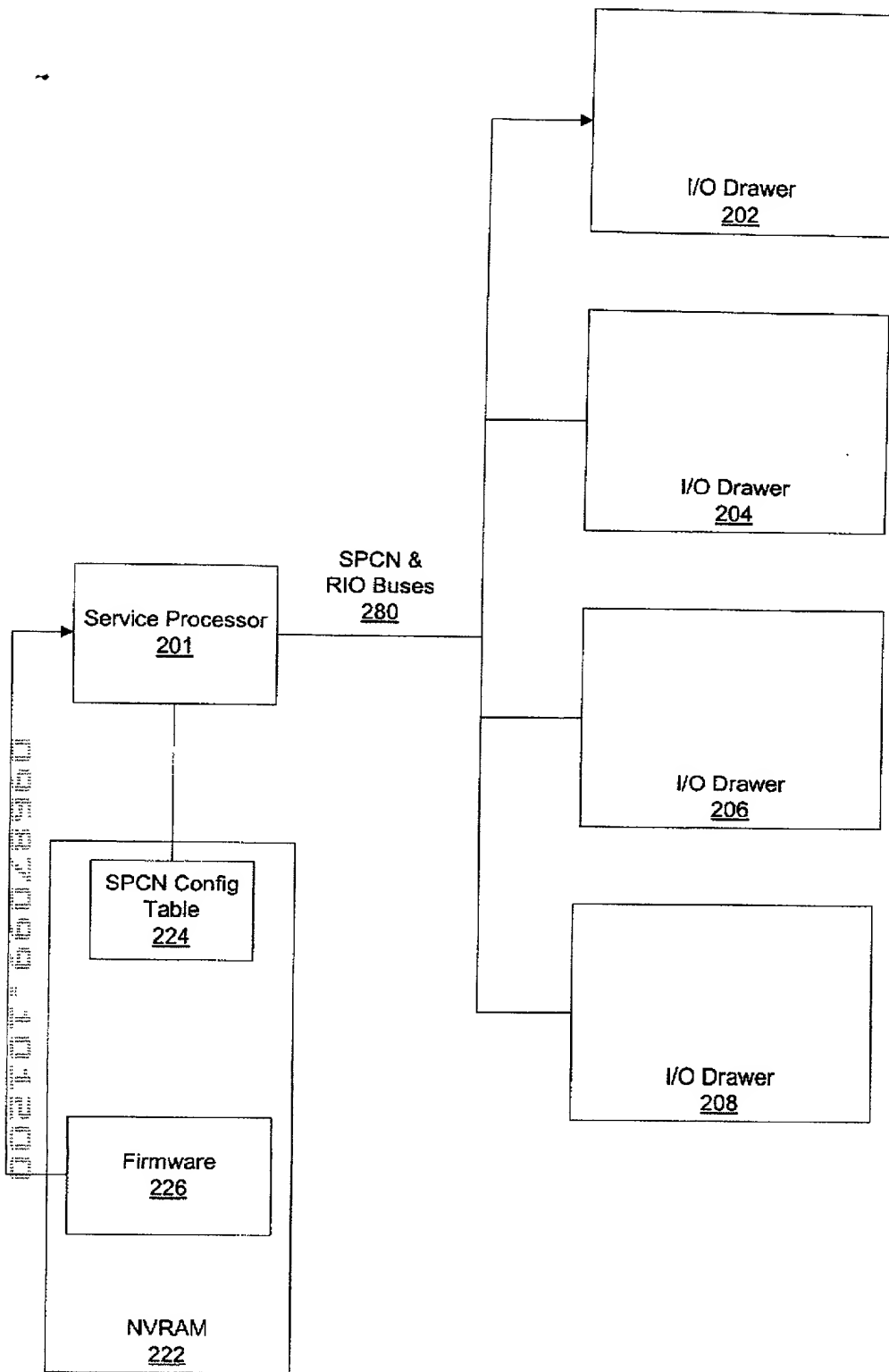
JTAG/I²C Busses
134

Processor
101

Processor
102

Processor
103

Processor
104

Memory
191

ATTN Signal

106
System Bus

Service
Processor
135

PCI Bus
195

Memory
Controller/
Cache
108

I/O Bridge
110

Service
Processor
mailbox
interface and
ISA Bus Access
Passthrough
194

ISA Bus
196

NVRAM
192

PCI/ISA Bridge
193

OP Panel
190

Local
Memory
160

Local
Memory
161

Local
Memory
162

Local
Memory
163

PCI Host Bridge
130

131
PCI Bus

EADS
132

133
PCI Bus

PCI I/O Adapter
136

I/O Bus 112

RIO
Controller
140

0   1   2   3

Bus
180

Bus
182

Bus
183

Bus
185

Bus
181

Bus
184

I/O Drawer
144

I/O Drawer
146

I/O Drawer
148

I/O Drawer
150

100
Data Processing System

Figure 1

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I/O Drawer
202

I/O Drawer
204

I/O Drawer
206

I/O Drawer
208

Service Processor
201

SPCN &
RIO Buses
280

SPCN Config
Table
224

Firmware
226

NVRAM
222

200
System

Figure 2

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Begin

Power on the system.
302

Service processor generates SPCN config table with all the drawers in the system and write to NVRAM.
304

Service processor ensures that each drawer connected via SPCN network has unique permanent address.
306

Firmware continues boot and reads SPCN config table information from NVRAM.
308

Firmware collects RIO network address for each drawer connected via RIO network.
310

Firmware fills up the SPCN config table with RIO network drawer address.
312

Firmware writes modified SPCN config table to NVRAM.
314

Firmware determines whether all drawer addresses match?
316

NO → **Firmware sends mailbox to service processor to assign new drawer address.**
318

↓

Service processor assigns new permanent SPCN drawer address to drawers that don't match with RIO drawer address.
320

YES

End

Figure 3

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DECLARATION AND POWER OF ATTORNEY FOR

PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A METHOD OF SYNCHRONIZING MULTIPLE NETWORKS USING PERMANENT ADDRESSING SCHEME

the specification of which (check one)

X is attached hereto.

___ was filed on _____
    as Application Serial No._____
    and was amended on _____
                              (if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):   Priority Claimed

                                                                ___ Yes___ No
_____ _____ _____
  (Number)   (Country)   (Day/Month/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ _____ _____
(Application Serial #)   (Filing Date)   (Status)

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I hereby declare that all statements made herein of my own knowledge are true
and that all statements made on information and belief are believed to be
true; and further that these statements were made with the knowledge that
willful false statements and the like so made are punishable by fine or
imprisonment, or both, under Section 1001 of Title 18 of the United States
Code and that such willful false statements may jeopardize the validity of the
application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following
attorneys and/or agents to prosecute this application and transact all
business in the Patent and Trademark Office connected therewith.

John W. Henderson, Jr., Reg. No. 26,907; Thomas E. Tyson, Reg. No. 28,543;
James H. Barksdale, Jr., Reg. No. 24,091; Casimer K. Salys, Reg. No. 28,900;
Robert M. Carwell, Reg. No. 29,499; Douglas H. Lefeve, Reg. No. 26,193;
Jeffrey S. LaBaw, Reg. No. 31,633; David A. Mims, Jr., Reg. 32,708; Volel
Emile, Reg. No. 39,969; Anthony V. England, Reg. No. 35,129; Leslie A. Van
Leeuwen, Reg. No. 42,196; Christopher A. Hughes, Reg. No. 26,914; Edward A.
Pennington, Reg. No. 32,598; John E. Hoel, Reg. No. 26,279; Joseph C. Redmond,
Jr., Reg. No. 18,753; Marilyn S. Dawkins, Reg. No. 31,140; Mark E. McBurney,
Reg. No. 33,114; Duke W. Yee, Reg. No. 34,285; Colin P. Cahoon, Reg. No.
38,836; Stephen R. Loe, Reg. No. 43,757; Stephen J. Walder, Jr., Reg. No.
41,534; Charles D. Stepps, Jr., Reg. No. 45,880; and Stephen R. Tkacs, Reg.
No. P-46,430.

Send correspondence to: Duke W. Yee, Carstens, Yee & Cahoon, LLP, P.O. Box
802334, Dallas, Texas 75380 and direct all telephone calls to Duke W. Yee,
(972) 367-2001.

FULL NAME OF SOLE OR FIRST INVENTOR: Tam D. Bui

INVENTORS SIGNATURE:_____ DATE:_____

RESIDENCE: 10905 Buckthorn Drive
            Austin, Texas 78759

CITIZENSHIP: United States

POST OFFICE ADDRESS: SAME AS ABOVE

FULL NAME OF SECOND INVENTOR: Chetan Mehta

INVENTORS SIGNATURE:_____ DATE:_____

RESIDENCE: 10101 Treasure Island Drive
            Austin, Texas 78730

CITIZENSHIP: United States

POST OFFICE ADDRESS: SAME AS ABOVE

FULL NAME OF THIRD INVENTOR: Keng-Hiup Ng

INVENTORS SIGNATURE:_____ DATE: October 4th, 2000

RESIDENCE: 55 Jalan Batalong 2
           Off Jalan Kuchai Lama
           58200 Kuala Lumpur
                        Page 2 of 3
           Malaysia

DOCKET NUMBER: AUS9-2000-0390-US1

CITIZENSHIP: Malaysia

POST OFFICE ADDRESS: SAME AS ABOVE

FULL NAME OF FOURTH INVENTOR: Jayeshkumar M. Patel

INVENTORS SIGNATURE:_____ DATE:_____

RESIDENCE: 3504 Katzman Drive
            Austin, Texas 78728

CITIZENSHIP: United States

POST OFFICE ADDRESS: SAME AS ABOVE

FULL NAME OF FIFTH INVENTOR: Amir Simon

INVENTORS SIGNATURE:_____ DATE:_____

RESIDENCE: 1102 Prairie Ridge Trail
            Austin, Texas 78660

CITIZENSHIP: United States

POST OFFICE ADDRESS: SAME AS ABOVE

FULL NAME OF SIXTH INVENTOR: Kiet Anh Tran

INVENTORS SIGNATURE:_____ DATE:_____

RESIDENCE: 1402 Hunter Ace Way
            Cedar Park, Texas 78613

CITIZENSHIP: United States

POST OFFICE ADDRESS: SAME AS ABOVE

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DECLARATION AND POWER OF ATTORNEY FOR

PATENT APPLICATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name;

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

A METHOD OF SYNCHRONIZING MULTIPLE NETWORKS USING PERMANENT ADDRESSING SCHEME

the specification of which (check one)

X is attached hereto.

__ was filed on _____
as Application Serial No._____
and was amended on _____
(if applicable)

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s):   Priority Claimed

_____ _____ _____   ___ Yes___ No
       (Number)   (Country)   (Day/Month/Year)

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, §112, I acknowledge the duty to disclose information material to the patentability of this application as defined in Title 37, Code of Federal Regulations, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

_____ _____ _____
(Application Serial #)   (Filing Date)   (Status)

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

0ohn W. Henderson, Jr., Reg. No. 26,907; Thomas E. Tyson, Reg. No. 28,543; James H. Barksdale, Jr., Reg. No. 24,091; Casimer K. Salys, Reg. No. 28,900; Robert M. Carwell, Reg. No. 28,499; Douglas H. Lefeve, Reg. No. 26,193; Jeffrey S. LaBaw, Reg. No. 31,633; David A. Mims, Jr., Reg. 32,708; Volel Emile, Reg. No. 39,969; Anthony V. England, Reg. No. 35,129; Leslie A. Van Leeuwen, Reg. No. 42,196; Christopher A. Hughes, Reg. No. 26,914; Edward A. Pennington, Reg. No. 32,588; John E. Hoel, Reg. No. 26,279; Joseph C. Redmond, Jr., Reg. No. 18,753; Marilyn S. Dawkins, Reg. No. 31,140; Mark E. McBurney, Reg. No. 33,114; Duke W. Yee, Reg. No. 34,285; Colin P. Cahoon, Reg. No. 38,836; Stephen R. Loe, Reg. No. 43,757; Stephen J. Walder, Jr., Reg. No. 41,534; Charles D. Stepps, Jr., Reg. No. 45,880; and Stephen R. Tkacs, Reg. No. P-46,430.

Send correspondence to: Duke W. Yee, Carstens, Yee & Cahoon, LLP, P.O. Box 802334, Dallas, Texas 75380 and direct all telephone calls to Duke W. Yee, (972) 367-2001
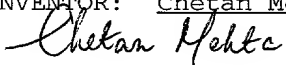
FULL NAME OF SOLE OR FIRST INVENTOR: Tam D. Bui

INVENTORS SIGNATURE: _____ DATE: 10/2/00

RESIDENCE: 10905 Buckthorn Drive
           Austin, Texas 78759

CITIZENSHIP: United States

POST OFFICE ADDRESS: SAME AS ABOVE

FULL NAME OF SECOND INVENTOR: Chetan Mehta

INVENTORS SIGNATURE: _____ DATE: OcTOBER, 2. 2000

RESIDENCE: 10101 Treasure Island Drive
           Austin, Texas 78730

CITIZENSHIP: United States

POST OFFICE ADDRESS: SAME AS ABOVE

FULL NAME OF THIRD INVENTOR: Keng-Hiup Ng

INVENTORS SIGNATURE: _____ DATE: _____

RESIDENCE: 1003 Rutland Drive, #210
           Austin, Texas 78758

CITIZENSHIP: <u>Malaysia</u>

POST OFFICE ADDRESS: <u>SAME AS ABOVE</u>

FULL NAME OF FOURTH INVENTOR: <u>Jayeshkumar M. Patel</u>

INVENTORS SIGNATURE: <u>Jayeshkumar M. Patel</u> DATE: <u>october 2, 2000</u>

RESIDENCE: <u>3904 Katzman Drive</u>
<u>Austin, Texas 78728</u>

CITIZENSHIP: <u>United States</u>

POST OFFICE ADDRESS: <u>SAME AS ABOVE</u>

FULL NAME OF FIFTH INVENTOR: <u>Amir Simon</u>

INVENTORS SIGNATURE: _____ DATE: <u>October 2, 2000</u>

RESIDENCE: <u>1102 Prairie Ridge Trail</u>
<u>Austin, Texas 78660</u>

CITIZENSHIP: <u>United States</u>

POST OFFICE ADDRESS: <u>SAME AS ABOVE</u>

FULL NAME OF SIXTH INVENTOR: <u>Kiet Anh Tran</u>

INVENTORS SIGNATURE: _____ DATE: <u>October 2, 2000</u>

RESIDENCE: <u>1402 Hunter Ace Way</u>
<u>Cedar Park, Texas 78613</u>

CITIZENSHIP: <u>United States</u>

POST OFFICE ADDRESS: <u>SAME AS ABOVE</u>